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DIGITAL PHASE MIXERS WITH ENHANCED SPEED

Background of the Invention

[0001] This invention relates to digital signal phase mixers. More particularly, this invention relates to digital phase mixers with enhanced speed.

[0002] A phase mixer typically receives two input signals and outputs a signal having a phase between the phases of the two input signals. Select signals can be used to determine the phase of the output signal. The number of bits in the select signals can indicate the number of possible intermediate phases, equally-spaced apart, that can be generated by the phase mixer. For example, two signals having a respective phase of 45° and 90° can be input to a phase mixer, which can then output a signal having a phase between 45° and 90°. If the select signals each have nine bits, the phase mixer can generate an output signal having one of eight possible intermediate phases (e.g., 50°, 55°, 60°, 65°, 70°, 75°, 80°, and 85°).

[0003] One voltage source typically drives the input signals, the select signals, and the output signal. Generation of the output signal, typically results in a

propagation delay, which increases the desired phase of the output signal. This non-zero propagation delay can impede the high speed performance of a phase mixer.

[0004] In view of the foregoing, it would be desirable to provide digital phase mixers with reduced propagation delay.

Summary of the Invention

[0005] It is an object of this invention to provide digital phase mixers with reduced propagation delay.

[0006] In accordance with this invention, the propagation delay is reduced by using two different voltage sources to drive a phase mixer. A first voltage source drives the input signals and the output signal, and a second voltage source, having a voltage higher than the first voltage source, drives the select signals. The higher voltage reduces the impedance of each transistor driven by the select signals, thus reducing the propagation delay at the output of the phase mixer.

[0007] In one embodiment, an elevated voltage source is applied to a non-differential digital phase mixer, reducing the propagation delay during the rising edges of the output signal.

[0008] In another embodiment, an elevated voltage source is applied to a differential digital phase mixer. In this embodiment, a more symmetric performance is achieved, reducing the propagation delay during both the rising and falling edges of the output signal.

[0009] The elevated voltage source can be any suitable voltage source. Often, several sources of different voltage levels are available in a system, any

one of which can be used as the elevated voltage source. For example, a pumped up voltage source (Vpp) used for a word line in a dynamic random access memory can be used as the elevated voltage source for the phase mixer.

Brief Description of the Drawings

[0010] The above and other objects and advantages of the invention will be apparent upon consideration of the following detailed description, taken in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout, and in which:

[0011] FIG. 1 is a block diagram of a phase mixer in accordance with the invention;

[0012] FIG. 2 is a circuit diagram illustrating a portion of the phase mixer of FIG. 1 in accordance with the invention;

[0013] FIG. 3 is a circuit diagram illustrating another embodiment of a phase mixer in accordance with the invention;

[0014] FIGS. 4-5 are timing diagrams of input and output signals of different embodiments of a phase mixer in accordance with the invention; and

[0015] FIG. 6 is a block diagram of a system that incorporates the invention.

Detailed Description of the Invention

[0016] The invention provides digital phase mixers with enhanced speed. FIG. 1 is a block diagram of one embodiment of a digital phase mixer in accordance with the invention. Phase mixer 100 receives two input signals 102 and 104 and two select signals 106 and 108,

and outputs a signal 116 having a phase between the phases of input signals 102 and 104. Input signals 102 and 104 can be clock signals, data signals, control signals, or other types of signals. Input signals 102 and 104 can have phases (e.g., 0°, 10°, 36°, 45°, 90°) that are any suitable degrees apart. (Although the invention is described herein primarily in the context of phase (e.g., with units of degrees or radians), the invention may also be described in the context of time (e.g., input signals 102 and 104 can be 100 picoseconds apart)). For more optimal performance, the maximum phase difference between input signals 102 and 104 is preferably less than about two to three times the total propagation delay time of phase mixer 100. The complement of select signals 106 and 108 (i.e., signals 106′ and 108′) can also be input to phase mixer 100. Alternatively, phase mixer 100 can include circuitry (e.g., inverters) that generates the complement of select signals 106 and 108. Select signals 106/106' and 108/108' can be generated by respective select drivers 120 and 122 or alternatively, by a single select driver.

[0017] Select signals 106 and 108 can each include N select bits that can be used to determine the phase of output signal 116 relative to the phases of input signals 102 and 104. N can be any reasonable number (e.g., 5, 10). The larger the value of N, the greater the number of possible intermediate phases that can be generated. However, having too large a value for N increases the amount of circuitry required for phase mixer 100 which can also increase the characteristic load of the circuitry, causing an undesirable change in the frequency of the output.

[0018] The select bits in select signals 106 and 108 can be directly related to each other. For example, in an ideal situation, if p out of N select bits are enabled in select signal 106 for input signal 102, then (N-p) select bits are enabled in select signal 108 for input signal 104. The greater the number of select bits enabled for input signal 102, the closer in phase output signal 116 is to input signal 102. The greater the number of select bits enabled for input signal 104, the closer in phase output signal 116 is to input signal 104. If the number of select bits enabled for input signals 102 and 104 are the same, the phase of output signal 116 will be substantially halfway between the phases of input signals 102 and 104. Although select signals 106 and 108 are described herein primarily in the context of separate signals 106 and 108 for clarity, one select signal can be input to phase mixer 100, which can then include circuitry (e.g., inverters) to generate the other select signal.

[0019] The phase relationship between input signals 102 and 104 and output signal 116 can be represented by the following equation:

$$\begin{aligned} \phi(OUT) &= \phi(IN_A)*(p/N) + \phi(IN_B)*(N-p)/N + \phi(T_{PM}) \\ &= \phi(IN_A)*K + \phi(IN_B)*(1-K) + \phi(T_{PM}) \qquad (1) \end{aligned}$$

ϕ = Phase
IN_A = First input signal 102
IN_B = Second input signal 104
OUT = Output signal 116
N = Number of select bits in select signals 106/108
p = Number of select bits enabled for the first input signal 102
K = p/N = Weighting factor for signal IN_A
1-K = Weighting factor for signal IN_B
T_{PM} = Propagation delay time

The phase of output signal 116 is the sum of three components. The first component is the phase of the first input signal 102 times its weighting factor (K). The weighting factor for input signal 102 is the number of select bits in select signal 106 that is enabled (p) divided by the total number of select bits (N). The second component is the phase of the second input signal 104 times its weighting factor (1-K). The weighting factor for input signal 104 is the number of select bits in select signal 108 that is enabled (N-p) divided by the total number of select bits (N). The third component is the phase of the total propagation delay (T_{PM}), which is determined by multiplying the total propagation delay by 360° (or $2\pi^{R}$) and dividing the result by the period of input signals 102 and 104. Although not shown, secondary factors may also affect the phase of output signal 116 including, for example, the sizing of the transistors used to implement phase mixer 100.

[0020] Phase mixer 100 includes two driving blocks 110 and 112 and an inverter 114. Input signal 102 and select signal 106 are input to driving block 110. Driving block 110 uses select signal 106 to produce an output with a phase that is proportional to the relative weight of input signal 102 to output signal 116. Input signal 104 and select signal 108 are input to a second driving block 112. Driving block 112 uses select signal 108 to produce an output with a phase that is proportional to the relative weight of input signal 104 to output signal 116. The outputs of driving blocks 110 and 112 are coupled such that the phases of the generated outputs are summed together and input to inverter 114. Inverter 114 inverts the logic

state of its input signal (i.e., from binary "1" to binary "0" or from binary "0" to binary "1") to produce output signal 116. A first voltage source (V_1) 130 is used to drive input signals 102 and 104, driving blocks 110 and 112, and inverter 114. A second voltage source (V_2) 140 is used to drive select drivers 120 and 122.

[0021] Each of driving blocks 110 and 112 can include the circuitry shown in FIG. 2. Driving block 200 receives an input signal 202 (e.g., signal 102 or 104), a select signal 204, and complement select signal 204' (e.g., signals 106/106' or 108/108'). Select signal 204 and its complement signal 204' can each have N select bits. Driving block 200 includes a driving unit 210. The number of driving units 210 can be the number of bits (e.g., N) in select signal 204 or other number. Each driving unit 210 includes two p-channel metal-oxide semiconductor (PMOS) transistors 212 and 214 and two n-channel metal-oxide semiconductor (NMOS) transistors 216 and 218 connected in series between a power voltage 220 and a ground voltage 222. The gate of PMOS transistor 212 is coupled to receive one of the bits of complement signal 204' while the source is connected to power voltage 220. The gate of NMOS transistor 218 is coupled to receive a corresponding bit of select signal 204 while the source is connected to ground voltage 222. The gates of PMOS transistor 214 and NMOS transistor 216 in each driving unit 210 are coupled to an input node 202 while the drains are tied to an output node 224. (A signal received at node 202 will hereinafter be referred to as

signal 202 while a signal output from node 224 will hereinafter be referred to as signal 224.)

[0022] In accordance with the invention, two different voltage sources are used. A first voltage source (e.g., voltage V_1 130, power voltage 220) is used to drive input signal 202 and output signal 224. A second voltage source (e.g., voltage V_2 140), having a voltage higher than the first voltage source, is used to drive select signal 204 and complement signal 204' (e.g., the enabled select bits). Accordingly, select signal 204 and complement signal 204' have a higher logical 1 voltage than input signal 202 and output signal 224. The higher voltage reduces the impedance of each NMOS transistor 218 driven by select signal 204, thus reducing the propagation delay at the falling edge of output signal 224. Because output signal 224 is sent to inverter 114, the propagation delay of phase mixer 100 is therefore reduced at the rising edge of output signal 116. The elevated voltage source can be any suitable voltage source. There are often several sources of different voltage levels available in a system, any one of which can be used as the elevated voltage source. For example, a pumped up voltage source (Vpp) used for a word line in a dynamic random access memory can be used as the elevated voltage source for the phase mixer.

[0023] FIG. 3 illustrates a differential digital phase mixer 300 in accordance with the invention. Phase mixer 300 receives a first input signal 302, complement input signal 302', and a select signal 306 having N select bits. Phase mixer 300 also receives a second input signal 304, complement input signal 304', and a select signal 308 having N select bits.

[0024] Phase mixer 300 includes a block 310 of two NMOS transistors 312 and 314 connected in series, a block 320 of two NMOS transistors 322 and 324 connected in series, a block 330 which is the mirror image of block 310, a block 340 which is the mirror image of block 320, and two PMOS transistors 350 and 352. The number of blocks 310 and 330 can each be the number of bits (e.g., N) in select signal 306 or any other suitable number. The number of blocks 320 and 340 can each be the number of bits (e.g., N) in select signal 308 or any other suitable number.

[0025] In block 310, the gate of NMOS transistor 314 is coupled to receive one of the select bits of select signal 306 while the source is connected to a ground voltage 356. The gate of NMOS transistor 312 is coupled to receive first input signal 302 while the drain is coupled to the drain of PMOS transistor 350.

[0026] In block 320, the gate of NMOS transistor 324 is coupled to receive one of the select bits of select signal 308 while the source is connected to ground voltage 356. The gate of NMOS transistor 322 is coupled to receive second input signal 304 while the drain is coupled to the drain of PMOS transistor 350.

[0027] In block 330, the gate of NMOS transistor 334 is coupled to receive the same select bit from select signal 306 as NMOS gate 314 in block 310. The gate of NMOS transistor 332 is coupled to receive complement input signal 302' while the drain is coupled to the drain of PMOS transistor 352.

[0028] In block 340, the gate of NMOS transistor 344 is coupled to receive the same select bit from select signal 308 as NMOS gate 324 in block 320. The gate of NMOS transistor 342 is coupled to receive complement

input signal 304' while the drain is coupled to the drain of PMOS transistor 352.

[0029] The sources of PMOS transistors 350 and 352 are connected to a power voltage 354. The drains of PMOS transistor 352 and NMOS transistors 332 and 342 are tied to output node 360, which is used to drive the gate of PMOS transistor 350. (A signal output from node 360 will hereinafter be referred to as signal 360). The drains of PMOS transistor 350 and NMOS transistors 312 and 322 are tied to complementary output node 360', which is used to drive the gate of PMOS transistor 352. (A signal output from complementary output node 360' will hereinafter be referred to as complementary signal 360').

[0030] Although the invention is described herein primarily in the context of PMOS and NMOS transistors (e.g., in FIGS. 2 and 3), any suitable gate or combination of gates may be used to implement a phase mixer in accordance with the invention.

[0031] Similar to that described in connection with FIG. 2, two different voltage sources are used. A first voltage source (e.g., power voltage 354) is used to drive input signals 302 and 304, their respective complements 302' and 304', output signal 360, and its complement 360'. A second voltage source, having a voltage higher than the first voltage source, is used to drive select signals 306 and 308 (e.g., the enabled select bits). Accordingly, select signals 306 and 308 have a higher logical 1 voltage than input signals 302 and 304, their respective complements 302' and 304', output signal 360, and its complement 360'. Because phase mixer 300 uses differential circuitry, a more symmetric output signal 360 is achieved, resulting in a

reduced propagation delay in the rising edges and falling edges of output signal 360. The elevated voltage source can be any suitable voltage source.

[0032] FIG. 4 shows a timing diagram 400 illustrating the operation of an ideal phase mixer that has zero propagation delay. For example, suppose a first input signal IN_A (e.g., signal 102 or 302) has a phase of 90° and a second input signal IN_B (e.g., signal 104 and 304) has a phase of 180° such that the phase difference between the two input signals is 90°. Suppose also that two select signals (e.g., signals 106/108 or 306/308) each have four select bits (e.g., N = 4). With four select bits, a phase mixer (e.g., phase mixer 100 or 300) can generate an output signal that has the same phase as either one of the input signals or one of three intermediate phases (e.g., 112.5°, 135°, or 157.5°) If four select bits (e.g., p = 4) are enabled for the first input signal IN_A, the phase mixer can output the first input signal IN_A. If three select bits (e.g., p = 3) are enabled for the first input signal IN_A, and one select bit is enabled for the second input signal IN_B, the phase mixer can output a signal 402 having a phase (e.g., 112.5°) between the phases of the two input signals, but closer to the phase of the first input signal IN_A. If two select bits (e.g., p = 2) are enabled for the first input signal IN_A, and two select bits are enabled for the second input signal IN_B, the phase mixer can output a signal 404 having a phase (e.g., 135°) halfway between the phases of the two input signals. If one select bit (e.g., p = 1) is enabled for the first input signal IN_A, and three select bits are enabled for the second input signal IN_B, the phase mixer can output a

signal 406 having a phase (e.g., 157.5°) between the phases of the two input signals, but closer to the phase of the second input signal IN_B. If four select bits are enabled for the second input signal IN_B, the phase mixer can output the second input signal IN_B.

[0033] Although FIG. 4 is described herein primarily in the context of a phase mixer with two input signals 90° apart in phase and with select signals having four select bits (for clarity), the two input signals to the phase mixer can be of other degrees apart in phase and have other numbers of select bits.

[0034] FIG. 5 shows a timing diagram 500 illustrating the operation of an embodiment of a phase mixer having non-zero propagation delay in accordance with the invention. In an ideal phase mixer, the phase mixer can output a signal 502 having an intermediate phase with zero propagation delay (e.g., $\phi(T_{PM}) = 0$) such that $\phi(OUT) = \phi(IN_A)*k + \phi(IN_B)*(1-k)$. In a conventional, non-differential phase mixer that uses one voltage source, the phase mixer outputs a signal 510 whose rising edge is delayed from the ideal phase by a propagation delay time 512 and whose falling edge is delayed by a propagation delay time 514. Propagation delay times 512 and 514 can be the same or different.

[0035] In one embodiment of the invention, for a non-differential phase mixer that uses different voltage sources as shown in FIGS. 1 and 2, phase mixer 100 outputs a signal 520 whose rising edge is delayed from the ideal phase by a propagation delay time 522 and whose falling edge is delayed by a propagation delay time 524. The propagation delay time 522 in the rising edge of signal 520 is less than

the propagation delay time 512 in the rising edge of signal 510.

[0036] In another embodiment of the invention, for a differential phase mixer that uses different voltage sources as shown in FIG. 3, phase mixer 300 outputs a signal 530 whose rising edge is delayed from the ideal phase by a propagation delay time 532 and whose falling edge is delayed by a propagation delay time 534. The propagation delay times 532 and 534 in the respective rising and falling edges of signal 530 are less than the propagation delay times 512 and 514 in the respective rising and falling edges of signal 510. Propagation delay times 532 and 534 can be the same or different.

[0037] Phase mixers 100 or 300 can perform phase mixing for any suitable purpose such as, for example, for generating a signal having a particular phase that is not readily available in a given circuit, for fine tuning adjustments of an input signal, and for synchronizing output data with an external clock signal. Phase mixers 100 or 300 can be implemented as dedicated circuitry or as part of other circuitry. For example, phase mixers 100 or 300 can be implemented in a digital delay-locked loop circuit, a frequency multiplying digital delay-locked loop circuit, or another suitable circuit.

[0038] The circuits on which phase mixers 100 or 300 are implemented can be peripherals that are part of a semiconductor random access memory (RAM) such as dynamic RAM (DRAM) or a synchronous DRAM (SDRAM).

[0039] FIG. 6 shows a system that incorporates the invention. System 600 includes a plurality of DRAM chips 610, a processor 670, a memory controller 672,

input devices 674, output devices 676, and optional storage devices 678. Data and control signals are transferred between processor 670 and memory controller 672 via bus 671. Similarly, data and control signals are transferred between memory controller 672 and DRAM chips 610 via bus 673. One or more DRAM chips 610 include a phase mixer in accordance with the invention. Input devices 674 can include, for example, a keyboard, a mouse, a touch-pad display screen, or any other appropriate device that allows a user to enter information into system 600. Output devices 676 can include, for example, a video display unit, a printer, or any other appropriate device capable of providing output data to a user. Note that input devices 674 and output devices 676 can alternatively be a single input/output device. Storage devices 678 can include, for example, one or more disk or tape drives.

Note that the invention is not limited to DRAM chips, but is applicable to other integrated circuit chips that implement phase mixers in accordance with the invention.

[0040] Thus it is seen that digital phase mixers with reduced propagation delay using an additional elevated voltage source are provided. One skilled in the art will appreciate that the invention can be practiced by other than the described embodiments, which are presented for purposes of illustration and not of limitation, and the present invention is limited only by the claims which follow.